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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

STEVENS, THOMAS H

ART UNIT PAPER NUMBER

2123

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/787,290

Applicant(s)

WESTPHAL, JONATHAN

Examiner

Thomas H. Stevens

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09/12/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-12 were examined.

Section I: New Examiner

New Examiner

2. Tom Stevens is presiding over the prosecution in place of William Thomson.

Section II: Non-Final Rejection

Specification (Amendment)

37 CFR 1.121

3. The following is a quotation of the 37 CFR 1.121:

The full text of any replacement paragraph with markings to show all the changes relative to the previous version of the paragraph. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strikethrough cannot be easily perceived

4. The amendment submitted on 09/12/2005 is non-compliant to 37 CFR 1.121 since the changes were not indicated by underline and or strikethroughs.

Claim Objections

5. The Office suggest amending the limitation of "a vector space" in line 6 of claim 2 to reflect "the/said vector space" because it unknown if the second vector space is the first vector space.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 10-12 are rejected under 35 U.S.C. 101 because the claim is directed to neither a "process" nor a "machine," but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. *Id. at 1551*. Furthermore, the limitations are unclear as whether the invention is software only or software coupled to a computer-based platform. Clarification is requested.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1, 2, 4,5, 8,9, 10-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the logic" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 2 recites the limitation "the logic" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the target schema" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the ANS-space" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the i-point" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the other" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the original clauses" in line 15. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the midpoint" in line 19. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the component" in line 19. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the vector" in line 20. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the simplification" in line 21. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the relevant clauses" in line 22. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the final schema" in line 30. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the subsuming clause" in lines 38-39. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the resultant" in lines 56-57. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "the system" in lines 60-61. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "the logic" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claims 8 and 9 recite the limitation "the processing element" in line 2. There is insufficient antecedent basis for this limitation in the claim.

10. Claims 10-12 recite the limitation "the logic" in line 6. There is insufficient antecedent basis for this limitation in the claim.

11. The phrase "i.e." in claim 4 renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See M.P.E.P. 2173.05(d).

12. The phrase "etc." in claim 4 renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See M.P.E.P. 2173.05(d).

13. Claims 10-12 are rejected under 35 U.S.C. 112 2nd since these claims reflect a both an apparatus and the method steps. *In Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990)*, a claim directed to an automatic transmission work stand and the method steps of using it was held to be ambiguous and properly rejected under 35 U.S.C. 112, second paragraph.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

15. Claims 1-3 and 5-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Turrini and further rejected under 35 U.S.C. 102(b) as being anticipated by Jain et al. (See 02/25/2005 Final office action, pages 6-8, for details).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. Claims 1-7 rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own admission (i.e., specification (AOA)) in view of Pillage et al., (US Application 5,379,231) (hereafter Pillage). AOA and Pillage are analogous since they both teach logic circuits.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize the vector space of Pillage in the logic circuit of AOA because Pillage teaches a method to provide an improved method and apparatus for simulating behavior of a microelectronic interconnect circuit at higher speeds than conventional circuit simulators (Pillage: column 3, lines 19-21).

Claim 1. A method of designing logic circuits (Pillage: column 1, lines 6 and 7), comprising the steps of: representing the logic of a logic circuit (Pillage: column 5, lines 3-5) to be designed as points and vectors in a vector space (Pillage: column 21, lines 5 and 6); and using the points and vectors in a vector space (Pillage: column 21, lines 5 and 6) to simplify the logic of the logical circuit to a simpler form (AOA, specification, pg.

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24, 3rd paragraph with 4th paragraph, lines 4 and 5 “logical device” “simplification machine”); and designing the logic circuit using the simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 “logical device” “simplification machine”).

Claim 2. A method of designing logic circuits (Pillage: column 1, lines 6 and 7), comprising the steps of: representing the logic of a logic circuit (Pillage: column 5, lines 3-5) to be designed as points and vectors in a vector space (Pillage: column 21, lines 5 and 6); and using the points and vectors in a vector space (Pillage: column 21, lines 5 and 6) to simplify the logic of the logical circuit to a simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 “logical device” “simplification machine”); and using the simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 “logical device” “simplification machine”) to implement the logic circuit in hardware (Pillage: column 5, line 6).

Claim 3. A method of simplifying the logic circuits, comprising the steps of: representing the logic of a logical circuit (Pillage: column 5, lines 3-5) as points and vectors in a vector space (Pillage: column 21, lines 5 and 6); and modifying (Pillage: column 42, lines 43-44) the representation in vector space (Pillage: column 21, lines 5 and 6) using at least one process rule of a set of process rules (series of steps, thus imply a series of rules: Pillage: column 34, lines 25 and 26) to simplify the logic (AOA, specification, pg.

24, 3rd paragraph with 4th paragraph, lines 4 and 5 “logical device” “simplification machine”).

Claim 4. The method of claim 3 in which at least one process rule of a set of process rules consisting of one of the following process rules: represent in alternational normal schema; the target schema t , as a set of vectors; each vector clause or disjunct of t is a position vector with a O at one corner of a set of parallelograms made of propositional addresses to the I-point at the other; any two other outside vertices of such a parallelogram are implicants of t (AOA, specification: 11, paragraphs 1-2 and 6).

Claim 5. Apparatus for simplifying logic circuits, comprising: a processing element configured to represent the logic of a logical circuit (Pillage: column 5, lines 3-5) to be simplified as points and vectors in a vector space (Pillage: column 21, lines 5 and 6) and to use the points and vectors to simplify the logic of the logical circuit to a simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 “logical device” “simplification machine”).

Claim 6. The apparatus of claim 5 in which the processing element is an optical computer (AOA: pg. 24, paragraphs 3-4).

Claim 7. The apparatus of claim 5, in which the processing element is a digital computer (AOA: pg. 1, "Description of Related Art" section, line 11 "Digital computers are, of course, well-known.").

19. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own admission (i.e., specification (AOA)) in view of Pillage as applied to claim1 above, and further in view of Chan et al., (US Patent 6,262,812) (hereafter Chan).

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize Chan and Pillage in AOA because Chan teaches a method to maximize the dynamic range of image values output from the image adjustment system (Chan: column 1, lines 50-52).

Claim 8. The apparatus of claim 1 in which the processing element is an colorimetric computer (Chan: column 3, lines 46-48).

20. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own admission (i.e., specification (AOA)) in view of Pillage as applied to claim1 above, and further in view of Yount (US Patent 4,622,667).

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize Yount and Pillage in AOA because Yount teaches data processing to reduce safety hazards resulting from generic faults in the software or the processors (Yount: column 1, lines 10-12).

Claim 9. The apparatus of claim 1 in which the processing element (Yount: column 3, line 43) is an analog computer (Yount: column 2, line 16).

21. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own admission (i.e., specification (AOA)) in view of Pillage, and further in view of Eng (US Patent 6,145,117). AOA, Pillage and Eng are analogous since they all teach logic circuits.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize the vector space of Pillage and the electronic model design of Eng in the logic circuit of AOA because Pillage teaches a method to provide an improved method and apparatus for simulating behavior of a microelectronic interconnect circuit at higher speeds than conventional circuit simulators (Pillage: column 3, lines 19-21). Eng teaches a method that enhances existing top-down EDA systems by implementing an automatic performance design paradigm (Eng: column 3, lines 38-40).

Claim 10. A computer program product comprising (Eng: column 25, lines 60-65): a computer program (Eng: column 25, line 37) stored in memory (Eng: column 12, lines 31-32) medium, said computer program comprising (Eng: column 25, line 37) instructions for representing the logic of a logic circuit (Pillage: column 5, lines 3-5) to be designed as points and vectors in a vector space (Pillage: column 21, lines 5 and 6); and using the points and vectors in a vector space (Pillage: column 21, lines 5 and 6) to simplify the logic of the logical circuit to a simpler form (AOA, specification, pg. 24, 3rd

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paragraph with 4th paragraph, lines 4 and 5 "logical device" "simplification machine"); and designing the logic circuit using the simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 "logical device" "simplification machine").

Claim 11. A computer program product (Eng: column 25, lines 60-65), comprising: a memory element (Eng: column 12, lines 31-32); and a computer program (Eng: column 25, line 37) stored on said memory (Eng: column 12, lines 31-32) medium, said computer program (Eng: column 25, line 37) comprising instructions for representing the logic of a logic circuit (Pillage: column 5, lines 3-5) to be designed as points and vectors in a vector space (Pillage: column 21, lines 5 and 6); and using the points and vectors in a vector space (Pillage: column 21, lines 5 and 6) to simplify the logic of the logical circuit to a simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 "logical device" "simplification machine"); and using the simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 "logical device" "simplification machine") to implement the logic circuit in hardware (Pillage: column 5, line 6).

Claim 12. A computer program product (Eng: column 25, lines 60-65), comprising: a memory element (Eng: column 12, lines 31-32); and a computer program (Eng: column 25, line 37) stored on said memory (Eng: column 12, lines 31-32) medium, said computer program (Eng: column 25, line 37) comprising instructions for representing the logic of a logical circuit (Pillage: column 5, lines 3-5) as points and vectors in a vector space (Pillage: column 21, lines 5 and 6); and modifying (Pillage: column 42, lines 43-

44) the representation in vector space (Pillage: column 21, lines 5 and 6) using at least one process rule of a set of process rules (series of steps, thus imply a series of rules: Pillage: column 34, lines 25 and 26) to simplify the logic (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 "logical device" "simplification machine").

Section III: Response to Applicant's Arguments dated 06/29/2005

Abstract

22. Applicant is thanked for addressing this issue. Objection is withdrawn.

Specification (References)

23. Applicant is thanked for addressing this issue. Objection is withdrawn.

Claim Objection

24. Applicant is thanked for addressing this issue. Examiner Stevens concurs with Examiner Thomson's concern regarding the presentation of claim 4, that denotes syntaxes ("process rules" with their applicable subcategories "g1" "g2" etc.) which is not in proper claim form. Applicant must rid the claims of these categories/processes and translate them to their legal equivalence. The objection stands.

102 Rejection

25. Applicant has not traversed on the merits of the 102 rejections from the 02/25/2005 final office action, thus the rejection stands.

Correspondence Information


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

May 5, 2006

TS


Paul P. Rodriguez 5/12/06
Primary Examiner
Art Unit 2125-2123